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For your personal information

number : MC08008 date : 1980 AUG 27

title : H.F. S.S.B. Synthesiser Design Considerations using HEF4750/4751

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Mullard

laboratory report

from the:

Mullard application laboratory,
Mitcham, England.

28 OKT. 1980
unclassified

number: MC08008 date: 1980 AUG 27

project: pages: A1 ; R27 ;

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ABSTRACT

This report explains the design of synthesisers for h.f. s.s.b. applications using the HEF4750/4751 LOCMOS I.C.'s. The divider configurations which can be used, together with the choice of phase comparator and loop filter components are explained. Particular emphasis is placed upon the choice of speed-up ratio, and the use of the subtractor in the HEF4751 to account for I.F. offsets.

ADVIES 1980-11-06 OCTROOI d.d.	XX AV	GV		B		BL
OPGAVE 1980-10-28 MAMO d.d.	X AV	XX GV	X EI	B		BL

BM/PA

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MCO8008

H.F. S.S.B. SYNTHESISER DESIGN CONSIDERATIONS USING HEF4750/4751

1. INTRODUCTION

The HEF4750/4751 LOCMOS frequency synthesiser devices are particularly well suited to use in h.f. s.s.b. applications. Such synthesisers usually have high division ratios and low reference frequencies, and many of the features of the HEF4750 are of value in overcoming these difficulties. For example, the high gain phase comparator helps to overcome the low loop gain resulting from the high division ratio, giving a system which has good noise performance. Also, the auxiliary digital phase comparator can provide a useful increase in locking speed if it is operated at a frequency which is a multiple of the step size.

The HEF4751 Universal Divider also has a number of features which are attractive in h.f. s.s.b. applications. For example, the predominantly decimal organisation of the device helps to simplify the logic circuitry associated with the programming of such synthesisers - keyboard programming is one example which can easily be implemented without the use of a microprocessor. Another useful feature is the subtractor, which allows almost any i.f. frequency to be accounted for without the use of complex external circuitry.

This report explains the design considerations associated with the use of these devices in such synthesisers. It will be appreciated, however, that it is impossible to describe all possible synthesisers of this type - the contents of this report are intended only to provide guidelines which the reader must apply to his own requirements.

2. DECIDING UPON THE DIVIDER CONFIGURATION

The divider configuration is arrived at from a consideration of the receive frequency range to be covered, together with the i.f. frequency and the step size. These factors govern the number of decades of control

which are required, and the frequency range that the VCO must cover. For example, to receive 2 to 30MHz with an i.f. frequency of 35.4MHz, then the VCO must operate over the range 37.4MHz to 65.4MHz. If this coverage is required with a step size of 10Hz, then seven decades of control are required, i.e.

10's	of	MHz
1's	of	MHz
100's	of	kHz
10's	of	kHz
1's	of	kHz
100's	of	Hz
10's	of	Hz

Once the number of decades required has been arrived at (usually six for 100Hz steps and seven for 10Hz steps), then a divider configuration can be chosen. A single HEF4751 with one prescaler gives five decades of control, and each additional prescaler gives one further decade (this assumes that the internal C0b prescaler of the HEF4751 is set to divide by 10/11). In this case, the number of external prescalers which can be used is limited to two, and so no more than six decades of control are available with a single HEF4751. It follows therefore that 10Hz steps cannot be achieved using only one HEF4751, and a slave mode device is required, and since this provides two extra decades of control, there is obviously no point in using two prescalers (with one exception which is explained later).

To summarise, therefore, the divider configuration options available are as follows:-

10Hz steps - one external prescaler and one slave mode device (as in fig.1.)

100Hz steps - one external prescaler and one slave mode device (as in fig.2.)
or
two external prescalers (as in fig.3.)

The foregoing applies only to synthesisers which operate with the local oscillator (i.e. the VCO) wholly between 10MHz and 100MHz, which will almost always be the case. In the event of operation above 100MHz, due possibly to the use of a very high i.f. frequency, another decade of control is required, and this must always be supplied by using an additionalexternal prescaler. Thus, for operation above 100MHz, two external prescalers are always required. In fact, this restriction applies to any synthesisers in which operation above 90MHz is required, as the maximum input frequency of the HEF4751 is 9MHz. This is the exception referred to earlier.

Note that it is very bad practice to use a range of local oscillator frequencies which cross a decade boundary, as this requires digital circuitry which switches the synthesiser configuration. This can be done, but is usually prohibitively complex and will not be discussed here.

When two prescalers are used, the $\overline{SY}$ signal must be regenerated at one tenth of its original width to ensure correct operation of the fast prescaler. Figs 4 and 5 show two possible techniques of doing this. Fig. 4 shows a circuit which will regenerate the synchronising signal when an integrated 10/11 prescaler is used, while fig.5 is the logic diagram of a 10/11 prescaler with a regenerated sync.output. This latter circuit could be implemented with three or four standard logic packages, although obviously attention must be paid to the speed of operation required in relation to the logic family chosen. In any case, interfacing must be provided between any parts which are implemented in non-compatible logic types, and great care should be taken to ensure that such interfacing is sufficiently fast in operation.

Fig. 6 shows the prescaler circuitry of a synthesiser covering 2 - 30MHz with a 35.4MHz i.f. in 100Hz steps, and using the configuration of fig.3 (the two prescaler option). The maximum frequency present at the input to the second prescaler is 6.54MHz,which is within the capabilities of the standard range LOCMOS (operating at 10V) used to implement the second prescaler. The connection of the regenerated sync. signal and the FB1 signal is made via a simple resistive attenuator, while the interface in the ECL to LOCMOS direction is performed by a PNP transistor.

3. ACCOUNTING FOR THE I.F. OFFSET

The numbers which are actually programmed into the synthesiser are the result of a subtraction, or

$$N = N_A - N_B$$

where N = the number programmed into HEF4751

N_A = number entered on data A inputs

N_B = number entered on data B inputs

Obviously, in h.f. s.s.b. applications where the local oscillator always runs high, the i.f. frequency must be added to the receive frequency, and not subtracted from it. It is therefore necessary to subtract not the i.f. frequency itself, but the tens complement of the number which represents it. For example, with an i.f. frequency of 35.4MHz, and decade significance as follows (as in the configuration of fig.2)

D4	-	10's	of MHz
D3	-	1's	of MHz
D2	-	100's	of kHz
D1	-	10's	of kHz
Do	-	1's	of kHz

Then the programming to receive a frequency of 21.347MHz, would seem to be

D5	D4	D3	D2	D1	DO	
0	2	1	3	4	7	DATA A
9_1	6	4	6	0	0	DATA B
0	5	6	7	4	7	RESULT

The result is 56.747MHz, which is equal to 21.347 + 35.4MHz as required. Unfortunately, the NEF4751 does not allow this type of operation as shown above because the D5 entry on data B forces the device into slave mode operation. The correct procedure is to hardware '1' on data A during D5, as shown below:

D5	D4	D3	D2	D1	DO	
1	2	1	3	4	7	DATA A
0_1	6	4	6	0	0	DATA B
0	5	6	7	4	7	RESULT

This removes the borrow which is generated, and hence the result is the same, In fact, this "hardwired '1'" procedure can be used for any i.f. frequency below 100MHz; the receive frequency can never be higher than the tens complement of the i.f.frequency, as this implies that the local oscillator frequency must be above 100MHz.

In the dual prescaler case (e.g. the configuration shown in fig.3, this problem does not arise. Six decades of control are required, so all decades DO - D5 are used, and there is no "Zero Minus Nine and Borrow" entry as in the previous case (assuming the i.f. frequency is greater than 10MHz, which will usually be the case). Taking the configuration of fig.3 as an example, the significance of decades would be:

D5 - 10's of MHz
D4 - 1's of MHz
D3 - 100's of kHz
D2 - 10's of kHz
D1 - 1's of kHz
DO - 100's of Hz

To receive a frequency of, say, 18.4319MHz with an i.f. frequency of 35.4MHz, then the programming would be as follows:

D5	D4	D3	D2	D1	DO	
1	8	4	3	1	9	DATA A
6	4	6	0	0	0	DATA B
5	3	8	3	1	9	RESULT

This gives the correct result of 53.8319MHz, and, as before, this configuration will operate satisfactorily as long as the required local oscillator frequency does not exceed 100MHz.

It should be appreciated that the result of the subtraction is the most important number - as long as it has the correct number of significant figures (equal to the number of decades of control required), the number of figures in N_A or N_B is of little importance. For example, in the "hardwired 1" configuration described earlier, N_A actually has six significant figures, while only five decades of control are required. The subtraction of the data B information, however, always results in a five figure number, and the required equality is preserved.

There is another type of h.f. synthesiser which is occasionally used, in which the local oscillator frequency synthesised is the i.f. frequency minus the receive frequency. In other words increasing the receive frequency requires that the local oscillator frequency is decreased, as their sum is constant. The procedure in this case is to program the i.f. frequency on the data A inputs, and the receive frequency on data B. The number $N_A - N_B$ is therefore the local oscillator frequency as required. Unlike the previous cases, however, this arrangement can be used with i.f. frequencies greater than 100MHz. Suppose, for example, the i.f. frequency was 102MHz, and a receive range of 2 - 30MHz was to be covered in, say, 100Hz steps. The local oscillator range is 100 - 72MHz, (or, strictly speaking 99.9999 to 72.0000MHz). Six decades of control are required, and as the maximum frequency exceeds 90MHz, the two prescaler configuration of fig.3 must be used. It appears at first sight as if

a problem exists, because there is no 100MHz decade, D5 being the 10MHz decade. Operation is, however, such that, as long as the lowest receive frequency is restricted to 2.0001MHz, no problem arises - the most significant '1' on data A can be omitted. Consider, for example, the reception of a frequency of 16.4376MHz with a 102MHz i.f. The programming would be as follows:

D5	D4	D3	D2	D1	DO	
0	2	0	0	0	0	DATA A
1	6	4	3	7	6	DATA B
8	5	5	6	2	4	RESULT

The resulting frequency is the required 85.5624MHz. Obviously the process relies upon the generation of a borrow in the most significant decade - this in turn implies that the minimum receive frequency is:

$$f_{IF} - 100 \text{ MHz}$$

Where f_{IF} is the i.f. frequency. This is obvious, however, because of the requirement that local oscillator is less than 100MHz.

This configuration works equally well if the i.f. frequency is less than 100MHz, and if the single prescaler configuration is used. In the latter case, a 100MHz decade is available, and so the full i.f. frequency can always be entered, the restriction that the local oscillator frequency remains less than 90MHz still applies however, and this would restrict the minimum receive frequency to 12MHz (with f_{IF} = 102MHz). This configuration is therefore of limited use.

4. CHOOSING THE PHASE COMPARATOR COMPONENTS

The main phase comparator (PC1) of the HEF4750 can be used with a very high value of gain - this is particularly important in h.f. s.s.b. synthesisers where the high division ration reduces the loop gain quite drastically. It is therefore advisable to ensure that the value of PC1

gain used lies in the range 3 - 5kV/cycle. This gain Kø is governed by the values of timing components TRA and TCA. These are chosen using the formulae:

$$K_{\phi} = \frac{120 \quad (V_{DD} - V_{SS} - 3.2)}{TRA \qquad TCA \qquad f_{REF}} \quad \text{V/cycle}$$

or

$$K_{\phi} = \frac{20 \quad (V_{DD} - V_{SS} - 2.4)}{TRA \qquad TCA \qquad f_{REF}} \quad \text{V/cycle (LN1231 only)}$$

where TRA = 18k for LN1231
or 68k for all other versions

f_{REF} = synthesiser step size

TCB is usually about half the value of TCA, while TCC is ten times TCB. Note that these capacitors must be low leakage types.

5. DESIGNING THE LOOP FILTER

The loop filter is designed by modelling the synthesiser PLL as a continuous time third order system with three coincident poles at S = -W. Using a loop filter with transfer function:

$$F(S) = \frac{1 + S\tau_2}{1 + S\tau_3} \cdot \frac{1}{S\tau_1}$$

as shown in fig.7, where

$$\tau_1 = R_1 C_1$$

$$\tau_2 = R_2 C_1$$

$$\tau_3 = R_3 C_2$$

then we get the following expressions for these time constants

$$\tau_1 = \frac{3K_V \quad K_\phi}{N \quad W^2}$$

$$\tau_2 = \frac{3}{W}$$

$$\tau_3 = \frac{1}{3W}$$

In these expressions

K_V = VCO gain (rad sec^{-1} V^{-1})

K_ϕ = PCl gain (V rad^{-1})

N = design division ratio

= $(N_{min} . N_{max})^{\frac{1}{2}}$

N_{min} = Minimum division ratio

N_{max} = Maximum division ratio

W = loop natural angular frequency (rad sec^{-1})

It is worth mentioning that, although the model of the PLL used to evolve this design procedure is a greatly simplified one, the use of more sophisticated sampled data models has not produced loop filter design with significantly better performance. The simple continuous third order model is probably, therefore, an acceptable approximation for this purpose.

The choice of W is a matter of compromise. Too high a value will allow the VCO to be modulated by any reference breakthrough or pick-up from the phase comparators, so a reasonable amount of low-pass filtering must be maintained. Too low a value of W, however, will increase lock times - this can be particularly troublesome in systems with low reference frequencies. An acceptable compromise in most applications is to choose W such that:

$$W = 2\pi f_{REF} / 10$$

Given this value, one can calculate the values of τ_1, τ_2, and τ_3 and hence arrive at values for components R_1, R_2, R_3, C_1 and C_2.

One problem which often arises, particularly in the case where 10Hz steps are required, is that the value of τ_1 required is unacceptably large. For example, it is practically impossible to directly implement a time constant of 200 or 300 secs, bearing in mind that C_1 must be non-polarised. Such a value is not unreasonable, however, particularly if the VCO gain is very high. The effective value of this time constant can be increased, however, by cascading an attenuator with the loop filter. The transfer function of the cascade is then:

$$\frac{1}{A} \cdot \frac{1}{S\tau_1} \quad \frac{1 + S\tau_2}{1 + S\tau_3}$$

and so the effective value of τ_1 is A times higher, where A is the attenuation factor. This means that including an attenuator allows the actual value of time constant used to be decreased to allow

reasonable component values to be used. Fig.8 shows one possible way of connecting this attenuator, although this does rely heavily on very good decoupling of the op-amp non-inverting input.

To arrive at a value for R_4 (the resistor from the PC2 output to the loop filter), one must take into account the change in loop gain involved when this comparator is used. The gain of PC2 is 5V/cycle (when the HEF4750 is used with a 10V supply), and the division ratio is M times lower, where M is the speed-up ratio used. The loop gain is therefore a factor of:

$$\frac{M\, K_{\phi PC2}}{K_{\phi\ PC1}} \quad \text{times greater}$$

and so we must choose R_4 such that

$$R_4 = M \frac{K_{\phi\ PC2}}{K_{\phi\ PC1}} R_1$$

Where $K_{\phi\ PC1}$ = gain of comparator PC1

$K_{\phi\ PC2}$ = gain of comparator PC2 = 5V/cycle

If for example, $K_{\phi\ PC1}$ was 3000V/cycle and the speed up ratio was 10, then $R_4 = R_1/60$.

6. CHOOSING THE SPEED-UP RATIO (M)

Rather more constraint is placed upon the range of speed-up values available than is generally appreciated. The requirement that the capacitors TCA and TCB in the main phase comparator be completely discharged before another ramp is started on them places a limit on the speed-up ratio. It is difficult to be precise, but it is generally the case that the devices will not function properly if the speed-up

ratio is greater than about 50. Restricting oneself to decimal ratios, therefore, would seem to limit one to a value of 10. Indeed, with the decimal organisation of the HEF4751, it is expected that most customers using 10Hz or 100Hz steps will indeed use 10 times speed-up. It is, however, possible to use other ratios by abandoning the decimal organisation of the device, as the "tail end" counter of the HEF4751 is programmable (up to a modulus of 16), and there is also a half channel offset counter available. These facilities are fully described in Reference 1.

It seems unlikely, however, that the user will gain any advantage in terms of locking speed by increasing the speed-up ratio much above 10. The time taken to acquire lock is the sum of the time during which the system operates on PC2, and the time on PC1 - Obviously, increasing the frequency at which PC2 operates will reduce the time spent on this comparator, but the time required to lock on PC1 is constrained by the step size chosen, and cannot be reduced significantly. "Diminishing returns" therefore sets in rapidly once the speed up ratio is increased much above 10. It is recommended, therefore, that the decimal organisation is retained and a speed-up ratio of 10 is used.

7. CONCLUSIONS

The main considerations associated with the design of an h.f. s.s.b. synthesiser have been outlined. No attempt has been made to provide examples of circuitry peripheral to the synthesiser itself (e.g. programming circuitry), as this will vary widely with the requirements of the user.

8. REFERENCE

For a complete description of the HEF4750/4751 devices the reader is referred to:-

Giles,T.G., "Versatile LSI Frequency Synthesiser System", Mullard Technical Note 142, reprinted from "Electronic Components and Applications", Vol. 2, No.2, February 1980.

APPENDIX 1

LOOP FILTER DESIGN EXAMPLES

1. Design the loop filter for a synthesiser covering 2 - 30MHz with a 35.4MHz i.f., with 100Hz steps. The VCO gain is 3MHz/V, and the speed up ratio is 10.

Assuming the phase comparator gain is 3kV/cycle, we have:

$$K_\phi = 3000/2\pi \quad V\ rad^{-1},$$

$$K_V = 2\pi \times 3 \times 10^6 \quad rad\ sec^{-1}\ V^{-1}$$

The natural frequency of the loop is chosen to be one -tenth of the channel spacing i.e. 10Hz.

This $W = 2\pi \times 10 \quad rad\ sec^{-1}$

To determine N, consider the VCO range.

The oscillator actually covers:

$$2 + 35.4MHz - 30 + 35.4MHz$$

or $$37.4MHz - 65.4MHz$$

The step size is 100Hz, so the division ratio covers the range 374,000 - 654,000.

So, $$N = (N_{min}\ N_{max})^{\frac{1}{2}}$$

$$= (3.74 \times 10^5 \times 6.54 \times 10^5)^{\frac{1}{2}}$$

$$= 4.95 \times 10^5$$

Thus, $$\tau_1 = \frac{3K_V\ K_\phi}{N\ W^2}$$

$$= \frac{3 \times \frac{3000}{2\pi} \times 2\pi \times 3 \times 10^6}{4.95 \times 10^5 \times (2\pi \times 10)^2}$$

$$= 13.8 \text{ secs}$$

$$\tau_2 = \frac{3}{W}$$

$$= \frac{3}{\frac{\pi}{2\pi} \times 10}$$

$$= 47.7 \text{ Msecs}$$

and,

$$\tau_3 = \frac{1}{3W} = \frac{1}{9}\tau_2 = 5.3 \text{ Msecs}$$

Choosing $C_1 = 4.7\mu F$ then $R_1 = 2.93M\Omega$

and $R_2 = 10.14k\Omega$. Choosing $C_2 = 470nF$,

then $R_3 = 11.27k\Omega$

R_4 is given by

$$R_4 = \frac{5}{3000} \times M \times R_1, \quad \text{where } M = 10$$

$$= \frac{R_1}{60} = \frac{2.93 \times 10^6}{60}$$

$$= 48.8k\Omega$$

Taking the nearest preferred values to these, we have:

R_1 = 2.7MΩ

R_2 = 10kΩ

R_3 = 12kΩ

R_4 = 47kΩ

C_1 = 4.7μF

C_2 = 470nF

2. Design the loop filter for a synthesiser covering 1 - 28MHz with a 75MHz i.f., with 10Hz steps. The local oscillator frequency reduces as receive frequency increases. The VCO gain is 2.4MHz/V and the speed up ratio is 10.

The oscillator range is 74MHz to 47MHz, and the step size is 10Hz. The values of N_{min} and N_{max} are therefore:

$$N_{min} = 4.7 \times 10^6$$

$$N_{max} = 7.4 \times 10^6$$

Thus,

$$N = (4.7 \times 10^6 \times 7.4 \times 10^6)^{\frac{1}{2}} = 5.90 \times 10^6$$

The natural frequency of the loop is again chosen to be one-tenth of the reference frequency and is therefore 1Hz. So $W = 2\pi$ rad sec^{-1}.
Also, $K_V = 2\pi \times 2.4 \times 10^6$ rad sec^{-1} V^{-1}

and if we assume the phase comparator gain to be 4kV/cycle, then

$$K_\phi = 4 \times 10^3/2\pi \text{ V rad}^{-1}$$

Thus,

$$\tau_1 = \frac{3 K_v K_\phi}{N W^2}$$

$$= \frac{3 \times \frac{4000}{2\pi} \times 2\pi \times 2.4 \times 10^6}{5.90 \times 10^6 \times (2\pi)^2}$$

$$= 123.6 \text{ secs}$$

$$= \frac{3}{W} = \frac{3}{2\pi} = 477.5 \text{ Msecs}$$

and $$= \frac{1}{3W} = \frac{\tau_2}{9} = 53 \text{ Msecs}$$

Choosing C_1 to be 10μF, which is more or less the largest non-polarised capacitor one could reasonably expect to obtain, then,

$$R_1 = 12.36\text{MΩ}$$

$$R_2 = 47.75\text{kΩ}$$

Also with C_2 = 1μF, then R_3 = 53kΩ

Obviously 12MΩ is too high a resistor for R_1, and would in any case be very noisy. Its value must therefore be reduced using the attenuator technique. The value of R_4 must first be calculated, however.

$$R_4 = M \frac{K_{\phi\ PC2}}{K_{\phi\ PC1}} R_1 = 10 \times \frac{5}{4000} \times 12.36\text{MΩ}$$

$$= 154.5\text{kΩ}$$

To the nearest preferred values, then

R_2 = 47kΩ

R_3 = 56kΩ

R_4 = 150kΩ

C_1 = 10μF

C_2 = 1μF

The resistive attenuator preceding the loop filter can be chosen to have any reasonably large attenuation factor. Taking A = 120, then the value of R_1 required becomes approximately 100kΩ. The attenuator can be implemented with resistors

R_A = 1.2MΩ

R_B = 10kΩ

Where R_A and R_B are as shown in fig.8. Then the capacitor decoupling the non-inverting input of the op-amp must look like a very low impedance compared to 10kΩ at the loop natural frequency i.e. 1Hz. If we say that this capacitor must look like no more than 500Ω at this frequency, then

$$C > \frac{1}{2 \pi f R}$$

$$= \frac{1}{2 \times \pi \times 1 \times 500}$$

$$= 318\mu F$$

A suitable value for this decoupling capacitor would therefore be 330μF.

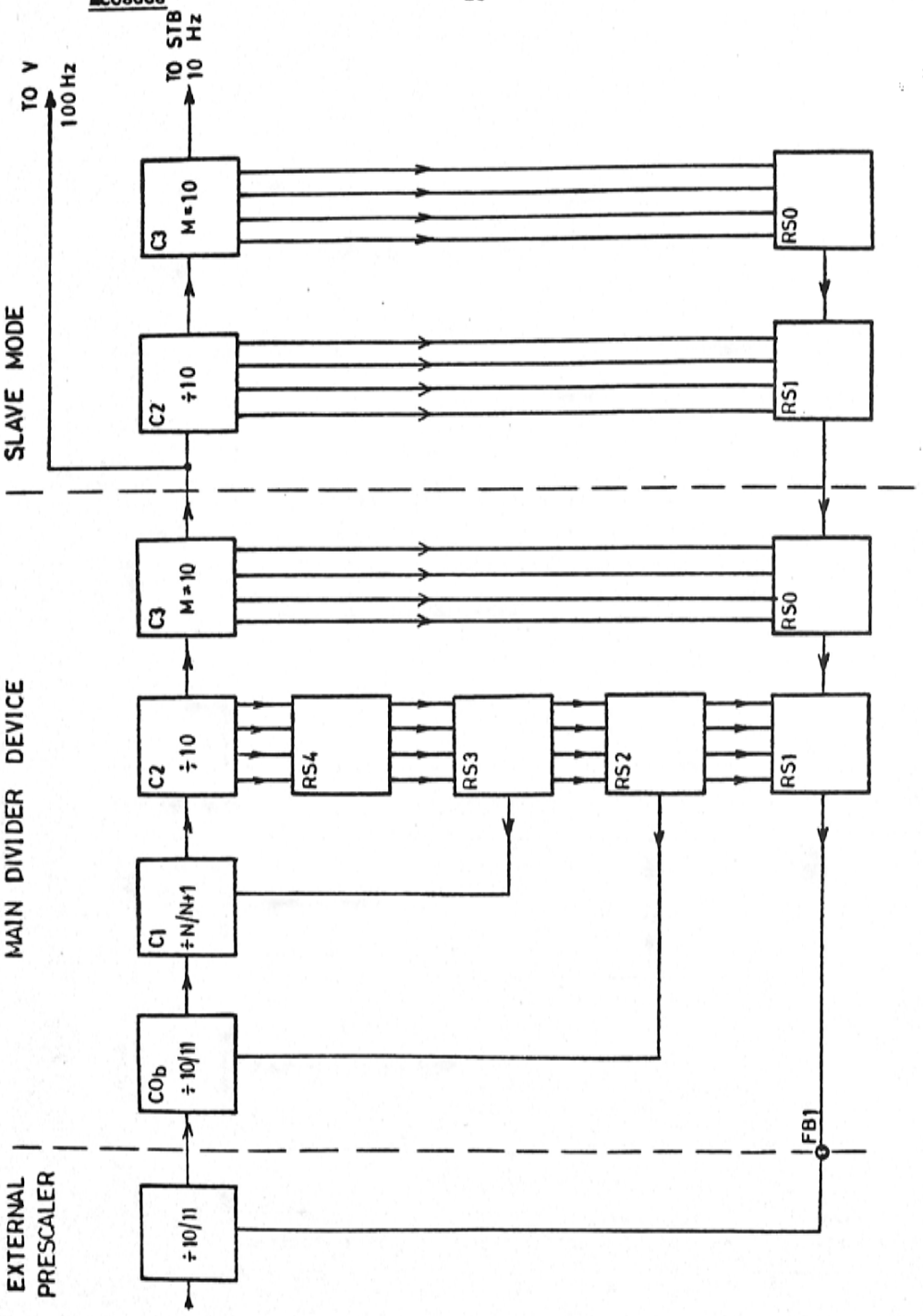

FIG. 1. DIVIDER CONFIGURATION FOR 10 Hz STEPS

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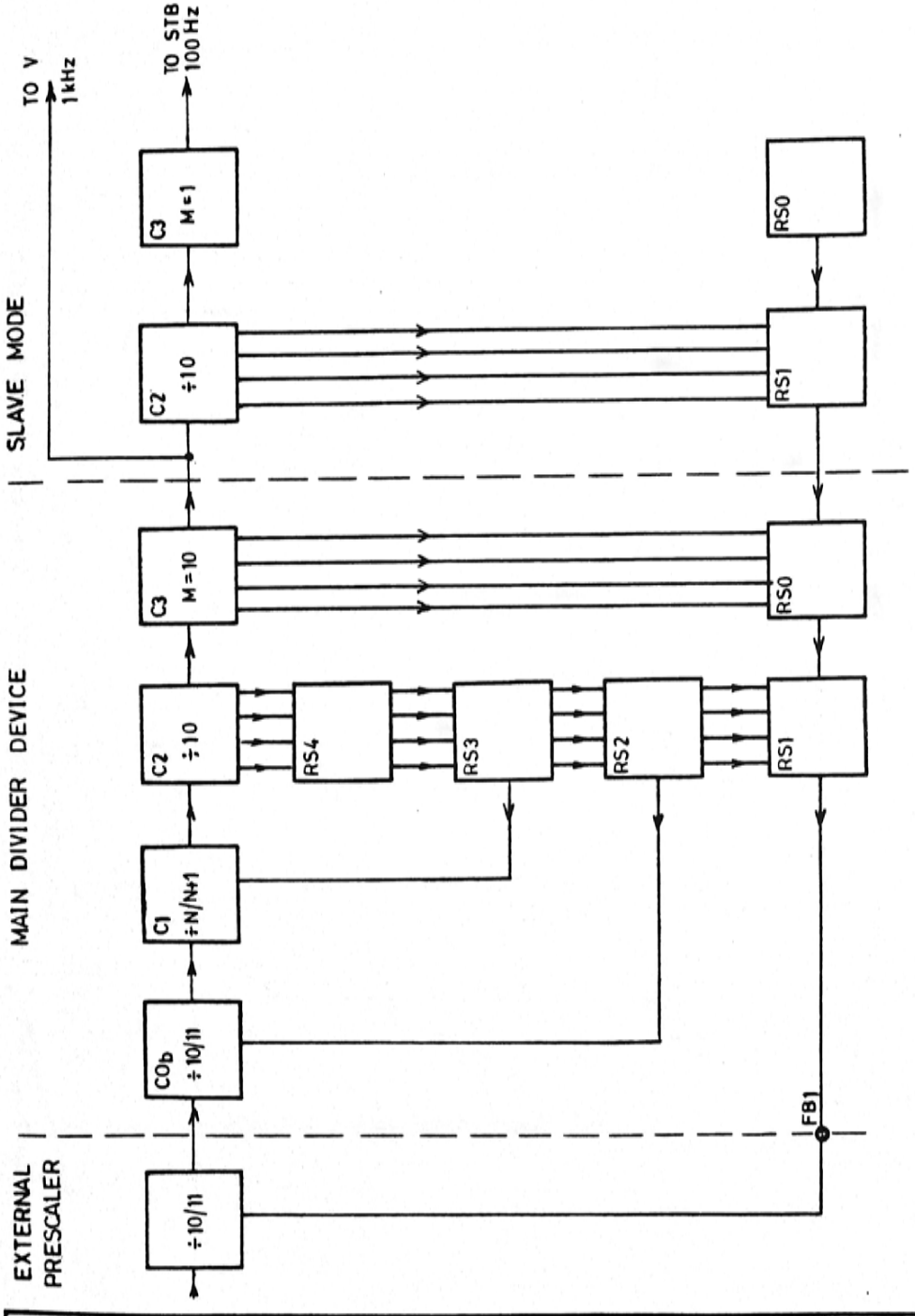


FIG.2 DIVIDER CONFIGURATION FOR 100Hz STEPS USING ONE EXTERNAL PRESCALER

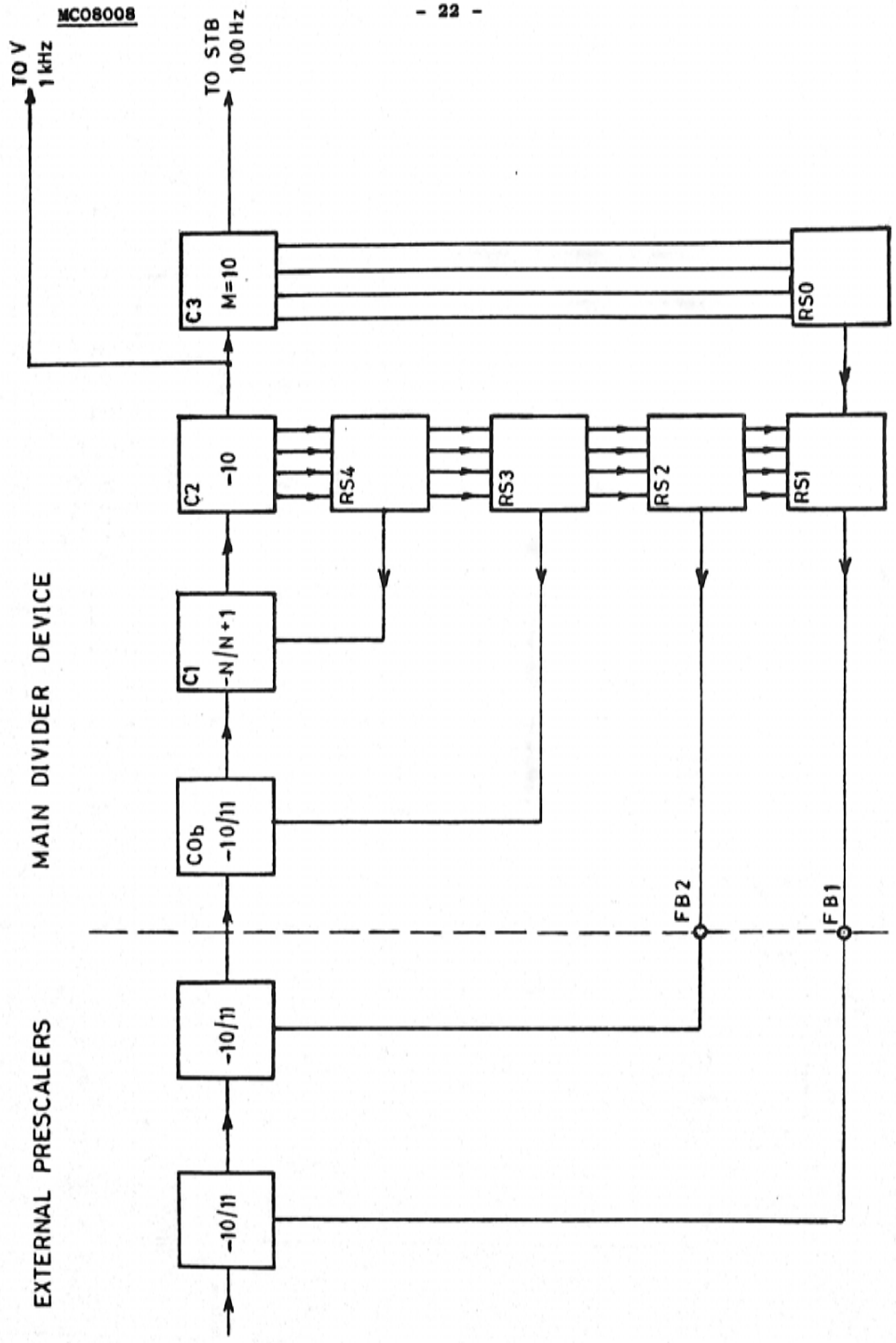
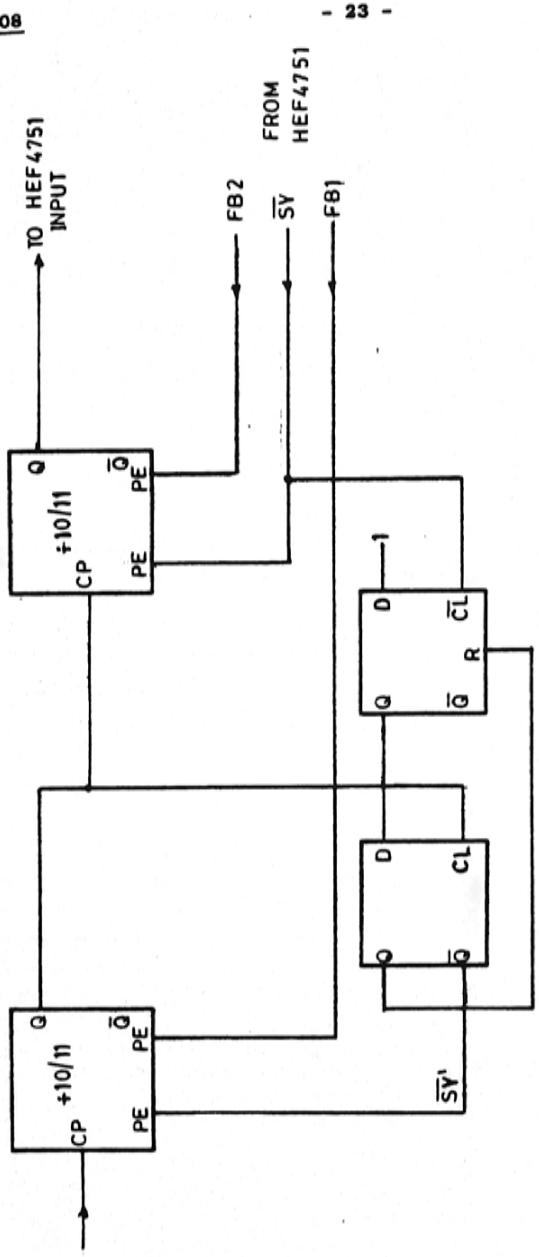


FIG. 3. DIVIDER CONFIGURATION FOR 100Hz STEPS USING TWO EXTERNAL PRESCALERS



$\overline{SY}$' IS THE REGENERATED SYNCHRONISING SIGNAL

FIG. 4. RESYNC CIRCUIT FOR INTEGRATED ÷10/11

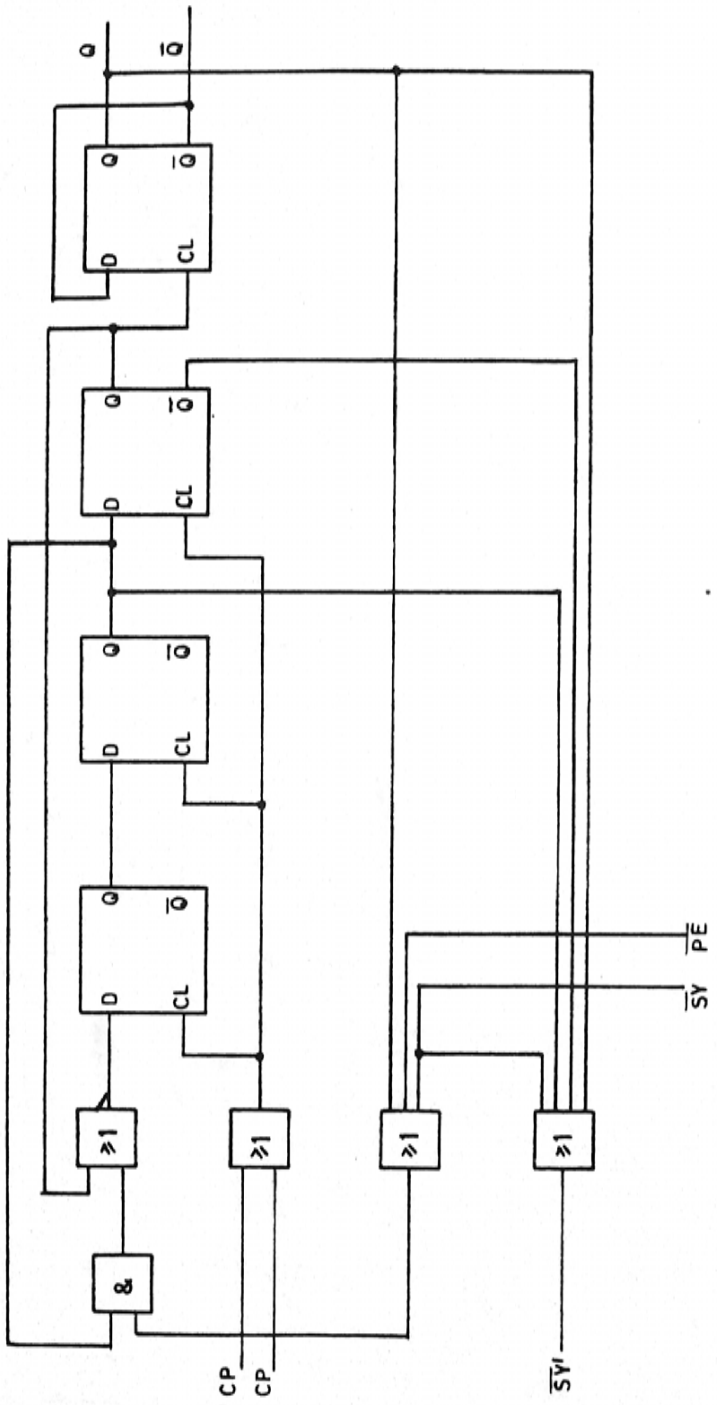


FIG. 5 ÷10/11 CIRCUIT WITH RESYNC GATING

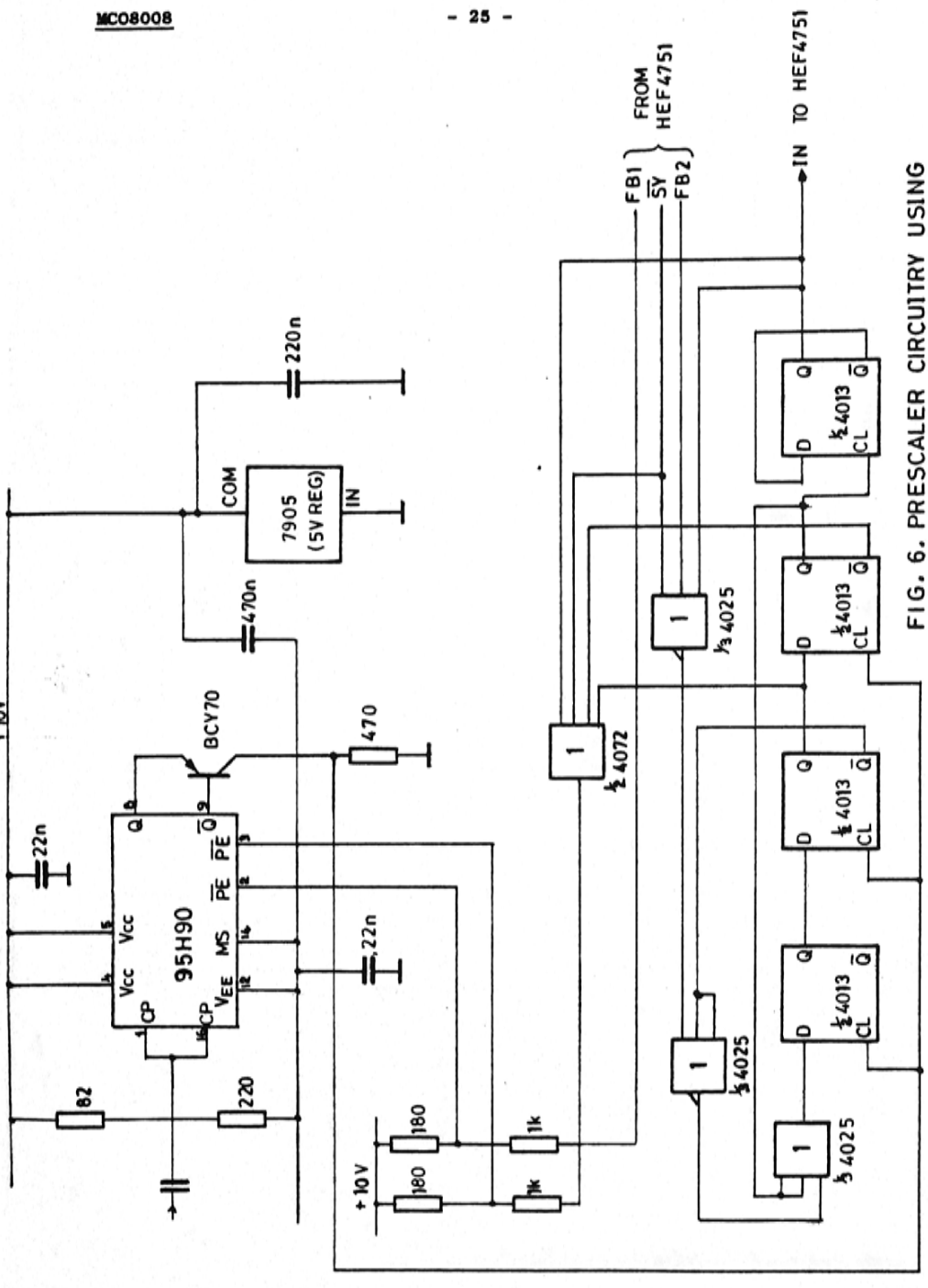


FIG. 6. PRESCALER CIRCUITRY USING DUAL PRESCALER CONFIGURATION.

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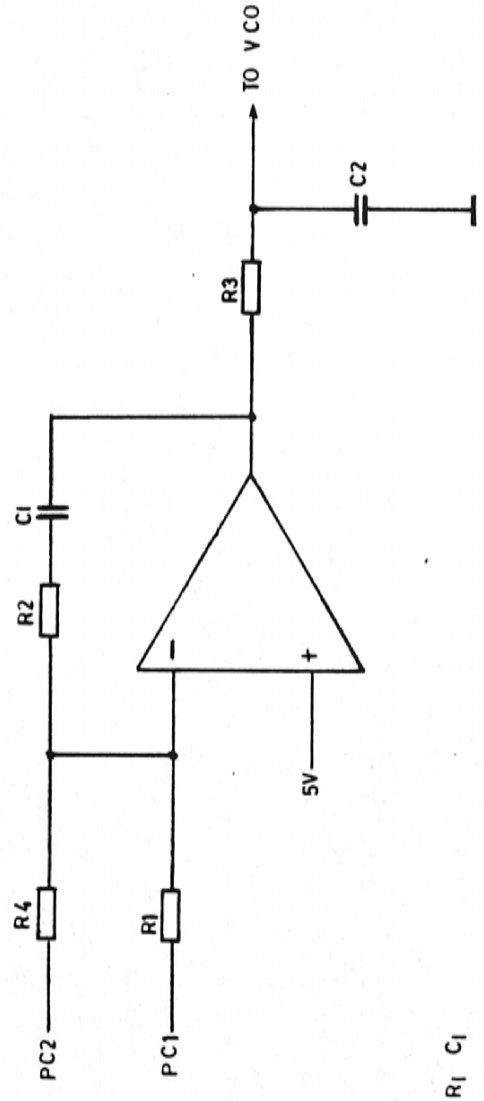

$\tau_1 = R_1 C_1$

$\tau_2 = R_2 C_1$

$\tau_3 = R_3 C_2$

FIG. 7. LOOP FILTER CIRCUIT

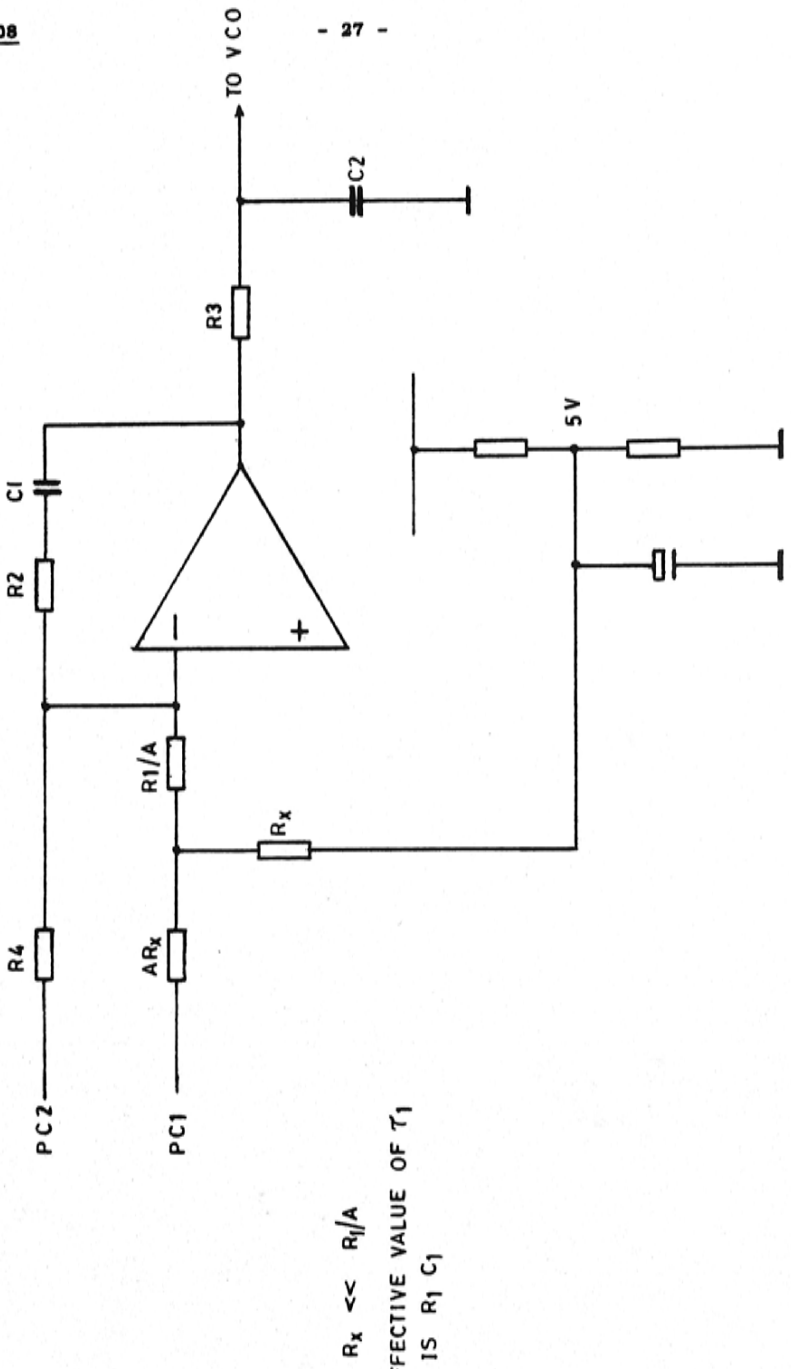

FIG. 8. ATTENUATOR TECHNIQUE OF INCREASING EFFECTIVE VALUE OF τ_1